PRR20

KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE
Opp : Yerragattu Gutta, Hasanparthy (Mandal), WARANGAL - 506 015, Telangana, INDIA.
काकतीय प्रौधोगिकी एवं विज्ञान संस्थान, वरंगल - ५०६ ०१५ तेलंगाना, भारत
కాకతీయ సాంకేతిక విజ్ఞాన శాస్త్ర విద్యాలయం, వరంగల్ - ౫౦౬ ౦౧౫ తెలంగాణ, భారతదేశం
(An Autonomous Institute under Kakatiya University, Warangal)
(Approved by AICTE, New Delhi; Recognized by UGC under 2(f) & 12(B); Sponsored by EKASILA EDUCATION SOCIETY)

ACADEMIC YEAR 2025-26: EVEN SEMESTER	
SCHEME: PRR20 II SEMESTER	
M.Tech. Embedded Systems & VLSI (ES&VLSI)	

Class Teacher: Sri G. Raju

DAY / TIME	09:40-10:30	10:30-11:20	11:20-12:10	12:10-01:00	L U N C H	02:00-02:50	02:50-03:40	03:40-04:30
MONDAY	ASCD	AICD	→Mini Project←			ESDWRTOS B-I-219	LVLSI B-I-219	LVLSI (T) B-I-219
TUESDAY	AICD	LVLSI	ESDWRTOS	ASCD	B R E A K	DM SH-3-1	-	-
WEDNESDAY	DM SH-3-1	ASCD	ESDWRTOS	AICD		-	-	-
THURSDAY	→ASCD Lab (B-I-217)← GR			ASCD (T)		DM SH-3-1	LVLSI B-I-219	ESDWRTOS(T) B-I-219
FRIDAY	→AICD Lab- (B-I-219)← BJ			AICD (T) B-I-219		-	-	-
SATURDAY	-	-	-	-		-	-	-

Course Title	Course Code & Course Name		Course Faculty
AICD	P20EV201: Analog IC Design	-	Dr. B. Jeevan (BJ)
ASCD	P20EV202: Advanced System On Chip Design	-	Sri G. Raju (GR)
LVLSI	P20EV203A: Low Power VLSI Design	-	Dr. K. Srinivas (KSC)
ESDWRTOS	P20EV204A: Embedded Systems Design with RTOS	-	Sri B. Venu Maheswar Rao (BVM)
DM	P20AC208D: Disaster Management	-	Dr. MD. Sameer
AICD Lab	P20EV205: Analog IC Design Laboratory	-	Dr. B. Jeevan (BJ)
ASCD Lab	P20EV206: Advanced System On Chip Design Laboratory	-	Sri G. Raju (GR)
Mini Project	P20EV207: Mini Project with Seminar	-	Dr. B. Jeevan (BJ)

Faculty I/c, *Dept. Timetables*	*Faculty I/c,* *Overall Timetables*	*Head of the Department*	*Dean, AA*	*Principal*